REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-21 in the application. In the present response, the Applicants have amended Claims 1, 6, 8, 13, 15, and 20. Support for the amendment can be found in paragraph 60 of the original specification. Additionally, Claim 2 has been amended to correct an inadvertent error. No other claims have been canceled or added. Accordingly, Claims 1-21 are currently pending in the application.

I. Rejection of Claims 1-14 under 35 U.S.C. §103

The Examiner has rejected Claims 1-14 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,578,137 to Parady in view of Microware's OS-9 White Paper. As argued below, the Applicants respectfully disagree in view of amended independent Claims 1 and 8.

As recognized by the Examiner, Parady does not teach a miss fulfillment FIFO or, based on a context switch request, storing a thread executing within a multi-thread execution pipeline loop in the miss fulfillment FIFO to prevent the thread from executing until a device request from the thread is fulfilled as recited in amended independent Claims 1 and 8. To cure this deficiency, the examiner cites OS-9. (*See* Examiner's Action dated August 7, 2006, pages 3-5.)

OS-9 provides a prioritized, round-robin scheduling algorithm with aging to allocate CPU time for processes. (*See* page 5.) In OS-9, a process that is running may yield for a specific condition to occur. Depending on what condition the process is waiting for, the yielded process is stored in one of several queues. (*See* page 5.)

None of the queues in OS-9, however, operate at a rate having a period associated with a pipeline latency of a multi-thread execution pipeline loop. On the contrary, OS-9 does not even

mention a multi-thread execution pipeline loop. Instead, operation of the queues of OS-9 is dependent on the round-robin scheduling algorithm. Thus, OS-9 does not teach or suggest storing a thread in a miss fulfillment FIFO until a device request is fulfilled, wherein the thread sequences through the entire miss fulfillment FIFO before exiting therefrom at a rate having a period associated with the pipeline latency of a multi-thread execution pipeline loop as recited in amended independent Claims 1 and 8.

The cited combination of Parady and OS-9, therefore, does not teach or suggest each and every element of amended independent Claims 1 and 8 and does not provide a *prima facie* case of obviousness of these independent Claims and Claims dependent thereon. Thus, Claims 1-14 are not unpatentable in view of Parady and OS-9. According, the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of Claims 1-14 and allow issuance thereof.

Furthermore, regarding amended dependent Claims 6 and 13, the cited combination of Parady and OS-9 does not teach or suggest a thread sequencing through a miss fulfillment FIFO at a rate equal to a pipeline latency of a multi-thread execution pipeline loop. As argued above, the cited combination does not even teach sequencing through a miss fulfillment FIFO at a rate having a period *associated* with a pipeline latency of a multi-thread execution pipeline loop.

II. Rejection of Claims 15-21 under 35 U.S.C. §103

The Examiner as rejected Claims 15-21 under 35 U.S.C. §103(a) as being unpatentable over Parady in view of U.S. Patent No. 5,509,006 to Wilford, *et al.* and in further view of OS-9. The Applicants respectfully disagree.

As discussed above regarding amended independent Claims 1 and 8, the cited combination of Parady and OS-9 does not teach or suggest storing a thread in a miss fulfillment FIFO until a device request is fulfilled, wherein the thread sequences through the entire miss fulfillment FIFO before exiting therefrom at a rate having a period associated with the pipeline latency as also recited in amended independent Claim 15. Wilford has been cited to teach tree engines that parse data. (*See* Examiner's Action dated August 7, 2007, page 9.) The Applicants do not find where Wilford cures the deficiencies of the cited combination of Parady and OS-9 in view of amended independent Claim 15 but is directed to providing a specialized apparatus capable of switching packets at high speed. (*See* Wilford, column 1, lines 65-66.) Thus, the cited combination of Parady, OS-9, and Wilford does not teach or suggest each and every element of amended independent Claim 15 and, as such, does not provide a *prima facie* case of obviousness of amended independent Claim 15 and Claims dependent thereon. Accordingly, the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of Claims 15-21 and allow issuance thereof.

Additionally, regarding amended dependent Claim 20, the cited combination of Parady and OS-9 does not teach or suggest a thread sequencing through a miss fulfillment FIFO at a rate equal to a pipeline latency of a multi-thread execution pipeline loop. As argued above, the cited combination does not even teach sequencing through a miss fulfillment FIFO at a rate having a period *associated* with a pipeline latency of a multi-thread execution pipeline loop.

III. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-21.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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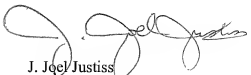

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